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15	2	6449629.URPN.	USPAT	2004/11/02 13:52
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-	571	carry and (complement$3 and (((sign or signed) and ((saturat$3 or scal$3) and (invert$3 and 708/$.ccls.))) and add$7))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/25 18:40
-	63	708/670-714.ccls. and (carry and (complement$3 and (((sign or signed) and ((saturat$3 or scal$3) and (invert$3 and 708/$.ccls.))) and add$7)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/25 18:40
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-	2	5957996.URPN.	USPAT	2003/11/25 19:06
-	6	("2823855" | "2799450" | "3083910" | "2872107" | "3584206" | "3571582").PN.	USPAT	2003/11/25 19:08
-	54	(9-bit$1 or (nine adj bit$1)) and 708/670-714.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/26 09:49
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-	7563	708/$.ccls. and parallel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/25 14:39
-	116	(708/$.ccls. and parallel) and VLIW	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/25 14:41

-	49	((708/$.ccls. and parallel) and VLIW) and (SIMD or MIMD)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/25 14:41
-	103	(saulsbury.in. and ashley.in.) or (rice.in. and daniel.in.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/11/01 13:17
-	2	(immediate$1 adj value$1) and ((saulsbury.in. and ashley.in.) or (rice.in. and daniel.in.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/11/01 13:35
-	2677	vliw	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/11/01 13:35
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